NRL Memorandum Report 4263

GaAs FET Device Fabrication and Ion Implantation Technology

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June 25, 1980

NAVAL RESEARCH LABORATORY
Washington, D.C.

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER (14) NRL-MR-4263	2. GOVT ACCESSION NO. AD-A087 004
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE *(and Subtitle)* GaAs FET DEVICE FABRICATION AND ION IMPLANTATION TECHNOLOGY	5. TYPE OF REPORT & PERIOD COVERED (9) Summary Report, 1 Oct 1978—30 Sept. 1979
6. PERFORMING ORG. REPORT NUMBER	
7. AUTHOR(s) (10) Kenneth J. Sleger and Harry B. Dietrich	8. CONTRACT OR GRANT NUMBER(s)
9. PERFORMING ORGANIZATION NAME AND ADDRESS Naval Research Laboratory Washington, D.C. 20375	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 62762N; ZF54-581-001; 52-0816-B-O
11. CONTROLLING OFFICE NAME AND ADDRESS (11) 25 Chief of Naval Material Command Washington, D.C. 20360	12. REPORT DATE June 1980
	13. NUMBER OF PAGES 25
14. MONITORING AGENCY NAME & ADDRESS *(if different from Controlling Office)* (12) 26	15. SECURITY CLASS. *(of this report)* UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*

Approved for public release; distribution unlimited.

(16) F54581

(17) ZF54581001

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

(18) SBIE

18. SUPPLEMENTARY NOTES

(19) AL-ECC 411

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

GaAs	Microwave field effect transistors
InP	Microwave semiconductor device
Ion implantation	Fabrication and evaluation

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

Microwave device fabrication and evaluation in conjunction with ion implantation has been selected to provide a benchmark technology for evaluation of semi-insulating GaAs and InP grown at NRL and elsewhere. Devices have been processed by a combination of conventional contact photolithography and liftoff techniques to achieve geometries with linewidths as small as 0.8 microns. A plasma deposited layer of Si_3N_4 has been employed as an annealing encapsulant at temperatures between 800°C and 850°C for 15—30 minutes

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20. Abstract (Continued)

(GaAs) or 700°C–750°C for 15 minutes (InP). Si and Se were used as the principal implant species. During this period, the Si_3N_4 encapsulation process and the fabrication of GaAs FETs with one micron gate lengths and noise figures below 2.4 dB at 6 GHz have become routine.

Both low level and high level Si implantation into GaAs and InP have been explored with encouraging results. Extended (8000Å) n type low level ion implanted layers in GaAs with activated free carrier concentrations as low as $3x10^{16}cm^{-3}$ have been achieved using NRL undoped semi-insulating GaAs substrates. These layers have been fabricated into the first all ion implanted GaAs TEDs. Ion implanted Si extended layers (3000Å) were also formed in NRL iron doped semi-insulating InP substrates. Here the lowest achieved carrier concentration was $1–2x10^{17}cm^{-3}$ as the result of the high iron level ($1–2x10^{16}cm^{-3}$) in the substrates. These layers were subsequently processed into the first all ion implanted InP TEDs which delivered as much as 106 mW of power at 2.1 GHz when operated as free running oscillators. High level Si ion implanted n^+ contacts were successfully employed on both InP and GaAs FETs and resulted in improvements in both noise figure and gain.

The most consistently good GaAs FET microwave performance was obtained using Se ion implantation into NRL undoped substrates to form the channel or with VPE channel layers grown on Cr doped semi-insulating substrates obtained from private industry. Noise figures as low as 1.7 dB at 6 GHz were obtained on the VPE channel GaAs FETs with one micron gate lengths while ion implanted channel GaAs FETs of equivalent geometry had noise figures about 0.5 dB higher at 6 GHz. Si ion implanted InP FETs displayed noise figures as low as 3.1 dB at 6 GHz. The first InP FETs with Se ion implanted channels were fabricated. For ion implanted FETs, the addition of the n^+ layer was found necessary to achieve the low noise figures quoted above.

Difference in microwave performance between ion implanted channel and epitaxial channel (industrially supplied) GaAs FETs was systemmatically correlated with various materials parameters such as mobility and light sensitivity and with static FET characteristics such as looping, backside gating, pinch-off voltage and transconductance. Experimental results indicate that good microwave performance can be obtained even though a few of the static or material characteristics are independently judged to be substandard.

TABLE OF CONTENTS

GaAs FET DEVICE FABRICATION AND ION IMPLANTATION TECHNOLOGY

INTRODUCTION

This report describes the NRL effort in providing a benchmark microwave device technology for characterizing the III-V compound semiconductor materials grown at NRL. The device test vehicle used for this purpose is the Schottky barrier field effect transistor (MESFET). In addition, a substantial amount of effort has been devoted to the use of ion implantation as a doping technology and as a means of improved materials control. At present, there is not a complete understanding of the relationship between III-V compound semiconductor microwave device performance and materials parameters, especially in the case of the MESFET.

The relationship of this effort to the entire NRL Electronic Material Technology Program has been previously discussed in Fig. 30 of NRL Memorandum Report 3701, (February 1978), and will not be elaborated upon in this report. Rather, emphasis will be placed on ion implantation and FET characterization results. Results on both GaAs and InP will be reported.

FET FABRICATION

Figure 1 shows a completed GaAs FET of the type exclusively used as a characterization vehicle during this reporting period. The gate length, l_g, is 0.8 - 1.5 microns while the gate width, W_g, is 300 microns. This FET geometry is popular in industry and thus offers a good standard of comparison by which to judge NRL microwave results. FET vertical geometry is shown in Fig. 2 with key dimensions indicated. The channel thickness, a, ranges from 1500Å to 3000Å depending on the channel doping. The channel vertical doping profile is obtained before FET fabrication using conventional C/V techniques. This information is used to determine the correct amount of gate recess necessary to achieve a given pinch-off voltage.

Manuscript submitted May 1, 1980.

FET processing proceeds using conventional contract photolithography and lifting of evaporated metal contacts. The region between the source and the drain is electrically isolated from the rest of the FET by chemically etching a mesa prior to source/drain, gate definition or by using neon bombardment after the source/drain are in place but before the gate is evaporated. A 2-3 μm layer of photoresist is used to protect the channel during the neon bombardment. The neon isolation technique is attractive since it represents a planar technology and allows for reproducible definition of 0.8 - 1.0 micron gate lengths. The gate recess trough is defined by chemical wet etching using a photoresist pattern as a mask. Some FETs employed ion implanted n^+ source/drain contacts. The n^+ layer was implanted over the entire water surface. For this case, a channel recess must be done to remove the highly conducting n^+ region from beneath the gate.

Source and drain contacts are evaporated Au/Ge/Ni alloyed at 450°C for 30 seconds and then overlaid with chromium-gold to aid in wire bonding. The gate is evaporated Cr/Au which is an attractive gate metallization because it adheres well to semiconductors and aids in wire bonding. Its disadvantage is that it is not reliable over a long period of time (years) unless a diffusion barrier metal such as platinum is inserted between the Cr and the Au. For the purposes of this program, Cr/Au gates are judged as acceptable and have yielded FETs with microwave performance comparable with that obtained in private industry.

ION IMPLANTATION

Ion implantation has been used to obtain state of the art small signal microwave GaAs FET performance at several industrial laboratories. In addition, ion implantation is the leading candidate for implementation of a SSI/MSI GaAs monolithic technology. In this program, ion implantation serves a dual role:

(1) as a semi-insulating GaAs qualification technique and materials characterization tool and (2) as a routine method of producing thin conducting layers on semi-insulating substrates suitable for fabrication into microwave devices. The integrity of GaAs semi-insulating substrates has been of vital concern to the microwave device community for roughly ten years and has provided the stimulus for this work at NRL. In a previous report, NRL Memorandum 4020, the problems associated with GaAs semi-insulating substrates are described and will not be repeated here.

The ion implantation effort at NRL is broad-based and deals primarily with the implantation of GaAs and InP. A portion of this effort funded under this program deals with evaluation of semi-insulating GaAs and InP supplied by NRL Code 6821. The work centers in three areas: encapsulation studies, developmental and routine implantation for FET fabrication and a study of low-level implantation suitable for TED devices.

During the past year, the NRL plasma deposited Si_3N_4 used for GaAs and InP encapsulation has been improved to the point where annealing of FET type implants ($n = 1x10^{17}cm^{-3}$, $x = 2500\text{Å}$) has become comparitively routine. The control of the encapsulation process for GaAs can be typified by recent data collected on a set of 20 Si implanted reference samples processed in 6 different runs over a period of ten weeks. The reference samples were all Cr doped, semi-insulating GaAs obtained commercially. The average Hall parameters for these samples were $N_s = 3.9x10^{12}cm^{-2}$ (45% activations) $\pm$ 19% and $\mu_H = 3900\ cm^2/V.sec \pm 5\%$. These samples were annealed at 850°C for 20 minutes. Two groups of Se implanted GaAs samples each containing four samples have also been processed. The average Hall parameters were $N_S = 5x10^{12}cm^{-2}$ (60% activation) $\pm$ 8% and $\mu_H = 4100\ cm^2$ (V.sec $\pm$ 5%). Typical annual time and temperatures were 20 minutes, 850°C, respectively.

Ion implantation has been used to produce channel regions for both GaAs and InP FETs. FET microwave performance is extremely sensitive to channel mobility, doping profile sharpness and substrate quality. GaAs FET results will be presented below in the paragraph entitled GaAs FET characterization results. Some results on InP FETs fabricated under another program, will be presented here. All of the implant work in InP has been done with either Si or Se in a single or double implant format. Some of the Si implanted InP FET profiles are shown in Fig. 3. These profiles were obtained from FAT FET test patterns which appear on the FET mask set and are processed exactly as are the microwave FETs. Consequently, the profiles of Fig. 3 reflect an 800Å gate recess for the double implant and no gate recess for the single implant. The primary purpose of the second implant is to provide an n^+ layer beneath the source/drain ohmic contacts. This is quite apparent from the double implant profile. Single dose Se implants ($3x10^{12}cm^{-2}$, 400 keV) produced profiles similar to that of the Si single implant in Fig. 3. Carrier Hall mobilities in the FET implanted regions ranged from 800-2600 $cm^2/V.sec$. InP FETs with the double implant profile shown in Fig. 3 had noise figures as low as 3.1 dB at 6 GHz with 8 dB associated gain. FETs employing the Si or Se single implant had best noise figures of 3.4 dB at 6 GHz with 7 dB associated gain. The larger noise figure of the single implant FETs presumably results from the lack of both the n^+ region and the recessed gate. The Se implanted InP FETs are the first of their kind.

A substantial effort was employed to explore low level implantation for possible use in planar GaAs TED structures. Such devices have been fabricated in private industry using vapor phase epitaxy to grow channels doped $1-2x10^{16}$ cm^{-3} anywhere from 0.5 - 1 microns thick. Such doping (n) - thickness (d) requirements are, in general, too stringent for ion implantation. The layer thicknesses are too great to be formed with conventional implantation equipment

and the doping concentrations are less than what can be obtained in the Cr doped semi-insulating GaAs substrates used by the industry. However, the nd, nl product requirements for TEDs can be met by increasing n tc say $5x10^{16}cm^{-3}$ and reducing d to say 0.3 microns. This may reduce device efficiency but allows ion implantation to be used for channel formation.

Using multiple implantation of Si, layers roughly 8500 hick can be obtained in GaAs with the NRL 300 KV implanter. The thickness d is defined as the depth at which the concentration is 10% of the maximum carrier concentration and the maximum implant energy is 600 keV (doubly ionized Si). For the work of this program 8500Å thick implanted Si layers of Atomic concentrations from $1x10^{16}cm^{-3}$ to $2x10^{17}cm^{-3}$ were used. From these, a comparison of the activations obtained in various types of semi-insulating GaAs substrates was made. The types of substrates are listed below:

Number	Source	Doping	Growth Method
1	NRL	Undoped	Liquid encapsulated Czochralski
2	Industrial	Cr	Boat Grown
3	Industrial	Cr with undoped buffer layer	Vapor Phase Buffer Layer

The following observations can be made to date. No n-type activity has been measured in any of the three types of material for implantation creating atomic layers of $2.7x10^{16}cm^{-3}$ or $1x10^{16}cm^{-3}$. The substrate with undoped buffer layer has only shown n type activity at atomic concentrations of $2x10^{17}cm^{-3}$, and although it has demonstrated activation as high as 50% with measured mobilities of 4300 $cm^2/V.sec$, it has not shown a consistent activation pattern even at this high concentration.

It has proven possible to obtain active layers with doping as low as $3x10^{16}$ cm^{-3} in the NRL undoped material. At atomic concentrations of $2x10^{17}cm^{-3}$

activations of 40% with mobilities of 4200 $cm^2/V.sec$ have been measured. At atomic concentrations of $8x10^{16}cm^{-3}$ activations of 60% and mobilities on the order of 3000 $cm^2/V.sec$ have been obtained. The lowest concentrations found to activate were $2x10^{16}cm^{-3}$. Figure 4 shows the calculated and measured profiles for such a sample. In contrast, the industrial Cr doped substrate showed no consistent pattern of activation at atomic concentrations at or below $8x10^{16}cm^{-3}$. Three terminal planar GaAs TEDs were fabricated and characterized under another program. NRL doped material with an activated ion implanted profile similar to that of Figure 4 was used. Current dropbacks of up to 23% were observed. Devices displayed negative resistance effects (free running oscillator) between 2 and 7 GHz. This represents the first all ion implanted planar GaAs TED.

Implants suitable for planar InP TEDs were also investigated. As a result of the relatively high iron background in NRL iron-doped semi-insulating InP substrates, n type activity could not be achieved much below $1x10^{17}cm^{-3}$ in those substrates. This value is 5-10 times higher than that considered optimum for planar TEDs. However, it was deemed worthwhile to fabricate TEDs using extended (3000Å) ion implanted layers with doping levels near $1x10^{17}cm^{-3}$. To achieve a uniformly doped extended layer, a triple Si implant was used. The resulting profile and implant parameters are shown in Fig. 5. The uncertainty in the measured profile (obtained by C/V technique) is about 20% and is due to fringing capacitance and a relatively leaky Schottky barrier diode. Planar 3 terminal TEDs were fabricated from this implanted material under another program. Current dropbacks as high as 35% were observed. Devices were mounted in microstrip carriers and evaluated as free running oscillators. The best result was a power output of 106 mW at 2.1 GHz with 6% efficiency. This is the first report of an all ion implanted planar InP TED.

GaAs FET CHARACTERIZATION - EXPERIMENTAL

The FET characterization sequence is shown in Figure 6. Note that signifi-

cant materials characterization is performed during the FET fabrication and that undesirable materials and/or processing parameters can be a cause for rejection. More details on the different types of characterization and accept/reject criteria can be found in NRL Memorandum Report 3701.

A variety of material was processed and an approximate wafer breakdown is indicated below:

WAFERS	CHANNEL	SUBSTRATE SOURCE
10	VPE (Industrial)	Industrial (Cr doped)
2	I^2 (Industrial)	Industrial (Cr doped)
4	I^2 (NRL)	Industrial (Cr doped)
12	I^2 (NRL)	NRL Code 6821 (undoped)

Some of the VPE industrial material employed a low doped buffer layer to improve the quality of the channel-substrate interface, presumably by reducing the out-diffusion of harmful impurities from the substrate into the channel. Several industrial laboratories have shown the addition of a buffer layer as a necessary condition to achieve low FET noise figure. Industrial results with ion implanted channels suggest that best results are obtained when implanting directly into a qualified substrate (non-coverting at high temperature) without a previously grown buffer layer. The NRL objective has been to provide semi-insulating GaAs of such quality that a buffer layer is unnecessary. The GaAs materials effort at NRL has centered on the growth of high purity undoped semi-insulating GaAs by the pyrolytic boron nitride encapsulation technique.[1] NRL ion implanted FETs fabricated on this material will be described in the next section.

GaAs FET CHARACTERIZATION RESULTS

Improvements in NRL FET process technology have resulted in routine processing of one micron gate length devices with noise figures less than 2.5 dB at 6 GHz, provided that the GaAs material is of "good"[2] quality. These noise figures

are more than 1 dB lower than those obtained one year ago and the best 6 GHz noise figures (1.7-1.8 dB) are no more than 0.4 dB above that theoretically predicted for the NRL FET geometry.[2] The best small signal performance is depicted in Fig. 7. The ion implanted FET was fabricated on NRL undoped semi-insulating GaAs (wafer #8) using a Se implant for the channel and a Si implant for n^+ ohmic contacts. The gate recess is not optimum on the ion implanted FET and this resulted in a relatively high source resistance (15-20 ohms) which reduced the transconductance and increased the noise figures. Had this non-optimum recess not occurred, it is believed that the noise figure would have been significantly lower than it was. Figures 8 and 9 show the doping profiles and the saturated velocity profiles, respectively for the FETs whose microwave performance is shown in Figure 6. Note the sharp roll off of the doping profiles and the high velocity almost to the interface with the substrate for both FET types. These characteristics are judged to be desirable and generally relate to outstanding microwave FET performance.

Of the various types of GaAs material that was processed, the most consistently good microwave performance was obtained from NRL undoped semi-insulating substrates (5-43-L) ion implanted with Se and from industrially supplied VPE channels grown with/without buffer layers on chromium doped semi-insulating substrates. However, a sufficient data base has not been generated to recommend the use of one type of channel formation techniques over another or the exclusive use of any one type of substrate material. The use of a buffer layer is still warranted in some cases; however, ion implantation directly into undoped semi-insulating substrates presents an attractive alternate to the buffer layer. The problem of sorting out these material parameters which distinguish a poor performing FET from a good performer are exceedingly complex and beyond the relatively small effort employed here. However, some general conclusions can

be drawn from the FET results obtained on various GaAs materials. In order to do this, it will be necessary to examine Tables 1 and 2 which list a variety of experimental parameters measured on FETs fabricated on different sources of material. All attempts were made to keep the processing parameters as uniform as possible from run to run except for the gate recess which was not used on all runs as indicated in Table 2. Table 3 gives additional information on ion implanted wafers 5 to 8. The tables suggest a clear trend in the relationship between the measured materials properties and microwave FET performance. FETs which have two or more of the properties judged undesirable to good FET performance (i.e., low mobility, looping, excessive light sensitivity, backside gating, I/V asymmetry, etc.) show substandard microwave performance. However, the presence of only a modest amount of one or two of these "undesirable" properties does not appear to dramatically degrade microwave performance.

An extreme case of undesirable materials properties occurred with wafer 4 supplied to NRL by an industrial vendor with an outstanding record of producing state of the art FET performance using similar type material. Some of the unused portion of this wafer was returned to the vendor who then applied state of the art processing techniques to produce FETs. FET microwave performance was disappointing, with noise figures at least 1 dB or more above those normally obtained. The vendor concurred with the NRL assessment of this wafer, but could offer no explanation as to the possible reason why the wafer was substandard.

ACKNOWLEDGEMENTS

The authors wish to express their gratitude to M. Bark and R. Corazzi for performing technical assistance in the areas of photolithography, wet etching and ion implantation. The InP TED fabrication was performed by Dr. Tung Weng of Oakland University, Rochester, Michigan, while at NRL on summer appointment and by one of the authors (K. J. Sleger). The GaAs TED fabrication was performed by Dr. Wallace Anderson of NRL. InP TED microwave circuit measurements

were performed by Mr. Eliot Cohen of NRL.

REFERENCES

1. Henry, R. L., and Swiggard, E. M., "LEC Growth of InP and GaAs Using PBN Crucibles," Gallium Arsenide and Related Compounds, 1978, Inst. of Phys. Conf. Series 33B (Institute of Physics, Bristol and London) 28, (1979).

2. Fukui, H., "Optimal Noise Figure of Microwave GaAs MESFETs," IEEE Trans. on Electron Dev., ED-26, 1032 (1979).

TABLE 1
CLASSIFICATION OF WAFER TYPES PROCESSED: MATERIALS PROPERTIES AND PHENOMENA

WAFER #	SUBSTRATE TYPE	CHANNEL TYPE	BUFFER TYPE	CHANNEL MOBILITY ($cm^2/V \cdot sec$)	LOOPS	DC LIGHT SENSITIVITY	BACKSIDE GATING	ASSYMETRY IN I/V
1	Cr doped Vendor A	VPE Vendor B	No	3600	No	No	No	No
2	Cr doped Vendor C	VPE Vendor D	No	4000	No	No	No	No
3	Cr doped Vendor A	VPE Vendor A	Yes	3600	No	No	No	No
4	Cr doped Vendor A	Ion Implanted Vendor E	No	2000	Acute	Acute	Acute	Acute
5	Cr doped Vendor F	Ion Implanted NRL	No	4100	Slight	Slight	Slight	No
6	Cr doped Vendor A	Ion Implanted NRL	No	2500	Moderate	Moderate	Moderate	Moderate
7	Undoped NRL 5-43-L	Ion Implanted NRL	No	3500	Slight	Slight	Moderate	Slight
8	Undoped NRL 5-43-L	Ion Implanted NRL	No		No	Slight	Slight	No

TABLE 2

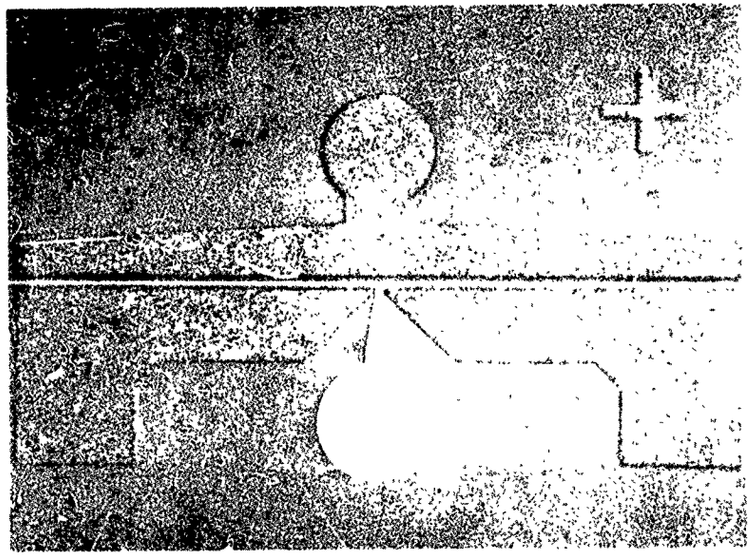
CLASSIFICATION OF WAFER TYPES PROCESSED: DC AND RF FET PERFORMANCE

WAFER #	CHANNEL TYPE	n^+ LAYER	GATE RECESS	I_{DSS}/gm mA/mmho	V_p VOLTS	6 GHz NOISE FIGURE dB	6 GHz ASSOCIATED GAIN dB	MINIMUM NOISE FIGURE BIAS V_{DS}/I_d Volts/mA
1	VPE Industrial	No	Yes	60-100/20-25	3-5	2.1-2.8	6-8	3.5/8
2	VPE Industrial	No	No	50-70/16-20	3-5	1.8-2.5	6-8	3/7
3	VPE Industrial	Yes	Yes	70-80/12-15	4-6	2.2-2.8	7-9	4/8
4	Ion Implant Industrial	No	Yes	7-12/12-15	0.5-0.6	5.0-5.8	5-6	4/3
5	Ion Implant NRL	No	No	35-50/12-15	3.0-3.2	2.8-3.5	7-8	3/8
6	Ion Implant NRL	No	No	30-35/18-20	2.5-2.8	3.0-3.5	6-8	3.5/8
7	Ion Implant NRL	No	No	25-45/18-20	2.5-3.0	3.0-3.5	6-7	4/8
8	Ion Implant NRL	Yes	Yes	18-25/10-15	2.0-2.2	2.2-2.8	7-8	4/4

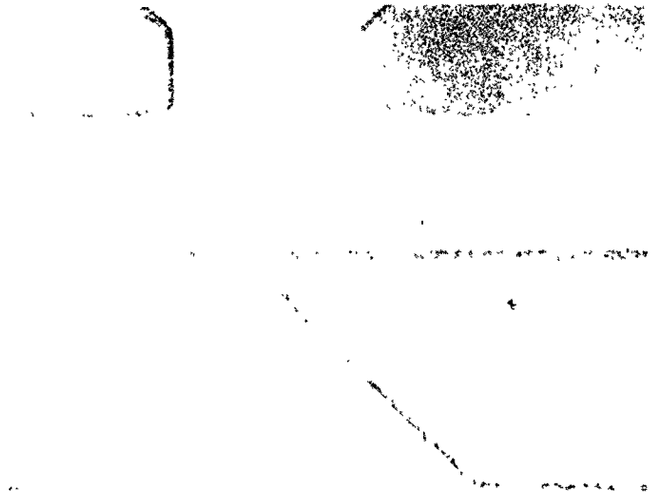
NOTE: All VPE material doped uniformly to $1x10^{17}cm^{-3}$
Standard $1x300\mu m^2$ FET geometry

TABLE 3
ION IMPLANTATION PARAMETERS FOR WAFERS 5 TO 8. IMPLANTATION DONE AT NRL WITH SOME CAPPING AT AFAL.

WAFER #	SUBSTRATE TYPE	IMPLANT ENERGY KeV	IMPLANT DOSE cm^{-2}	CAP TYPE	ANNEAL TEMP. °C	ANNEAL TIME °C	PEAK CARRIER CONCENTRATION cm^{-3}	AVERAGE ACTIVATED LAYER THICKNESS μm
5	Cr doped Vendor F	400	$4x10^{12}$ Se	Pyrolytic Si_3N_4 AFAL	850	20	$1.5x10^{17}$	0.3
6	Cr doped Vendor A	400	$3.5x10^{12}$	Pyrolytic Si_3N_4 AFAL	850	20	$1.5x10^{17}$	0.2
7	Undoped NRL 5-43-L	300	$3x10^{12}$ Se	Plasma Si_3N_4 NRL	850	20	$2x10^{17}$	0.3
8	Undoped NRL 5-43-L	300	$3x10^{12}$ Se	Plasma Si_3N_4	850	20	$1.6x10^{17}$	0.25
		20	$1x10^{13}$ Si	NRL	850	20	$\simeq 2x10^{17}$	< 0.1



(a) overall view of 1 μm x 300 μm NRL FET 400X



(b) close up of channel region near gate pad 1000X

Fig. 1 — NRL horizontal FET geometry at two different magnifications.
Optical photographs.

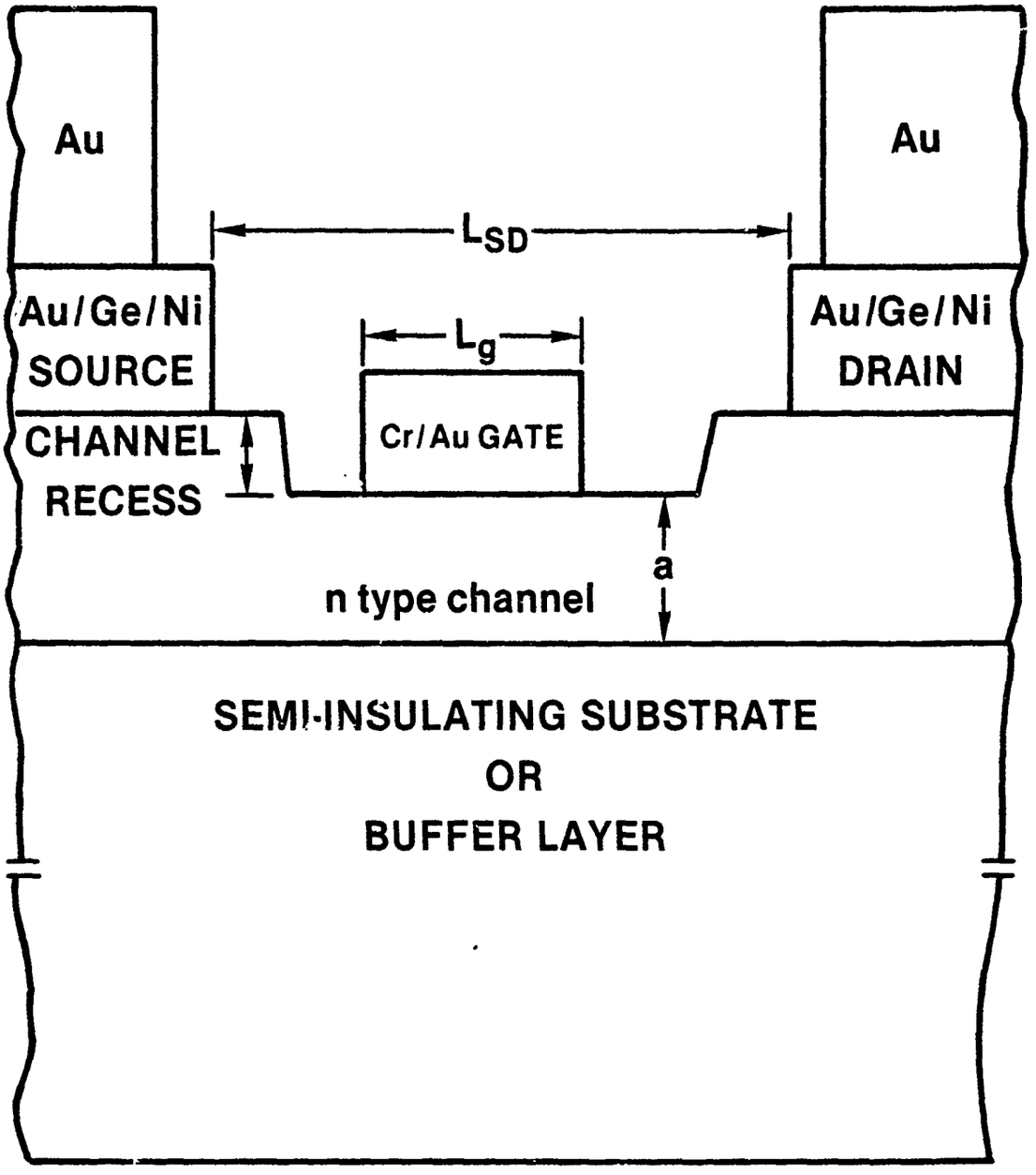


Fig. 2 — NRL vertical FET geometry showing key dimensions which affect microwave performance.

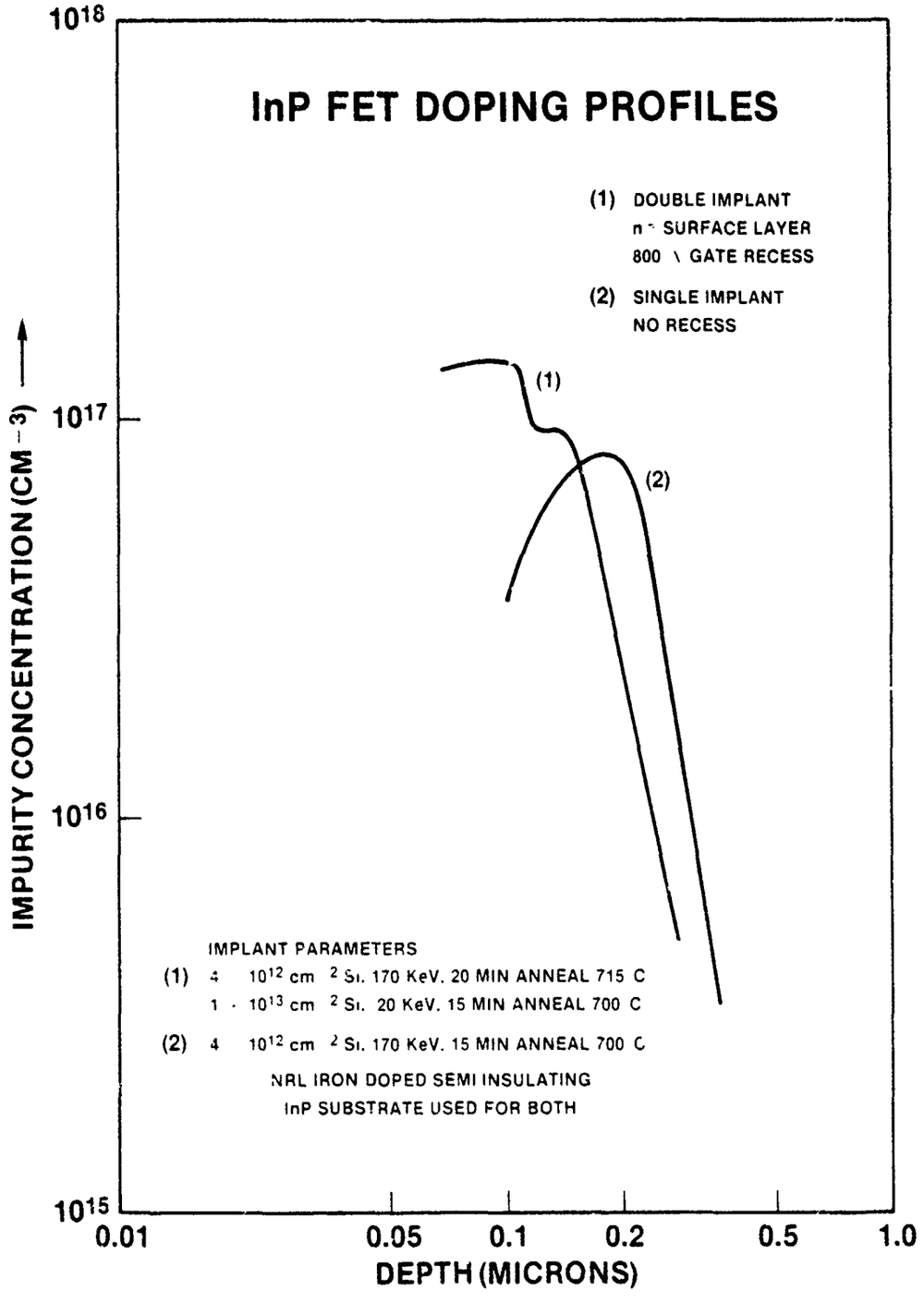


Fig. 3 — FET type ion implanted N/X profiles obtained on (100) oriented iron doped semi-insulating InP grown at NRL. Ion implantation performed by NRL Code 6812. Double implant provides n^+ layer under source/drain to reduce contact resistance and flatten profile beneath gate. Profiles obtained from FET mask test patterns.

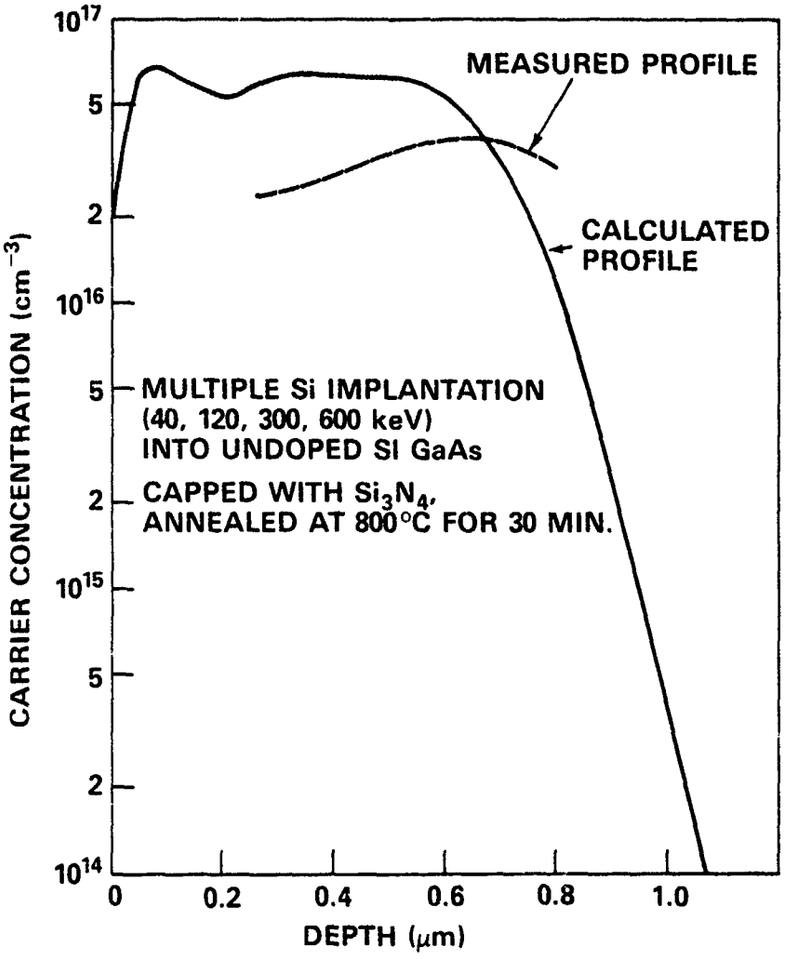


Fig. 4 — TED type ion implanted N/X profiles obtained on (100) oriented unintentionally doped semi-insulating GaAs grown at NRL. Ion implantation performed by NRL Code 6812. Multiple implant provides flat profile over 6000Å thickness.

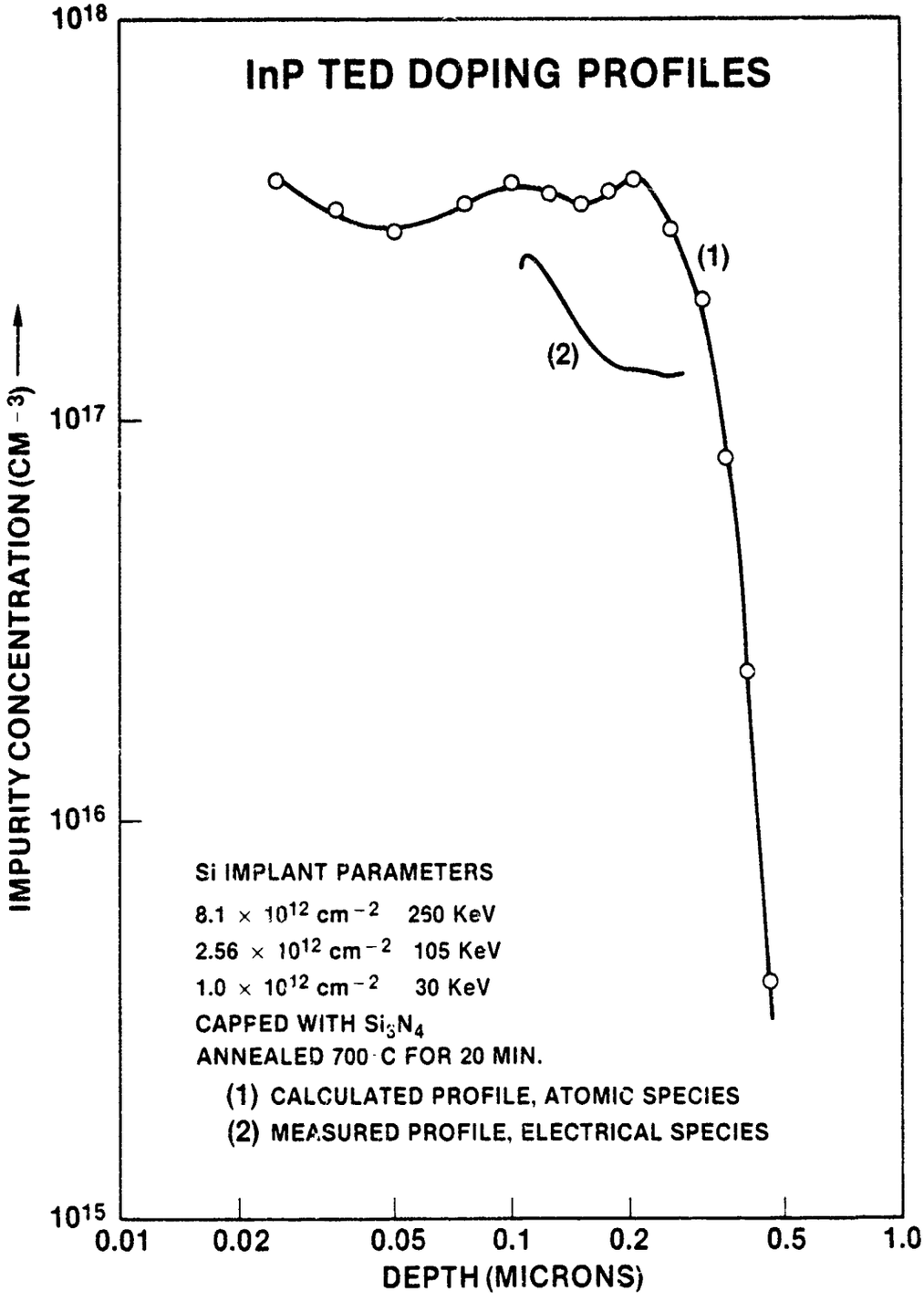


Fig. 5 — TED type ion implanted N/X profiles obtained on (100) oriented iron doped semi-insulating InP grown at NRL. Ion implantation by NRL Code 6812. Multiple implant provides flat profile over 3000Å thickness.

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GaAs FET FABRICATION AND CHARACTERIZATION
FLOW CHART

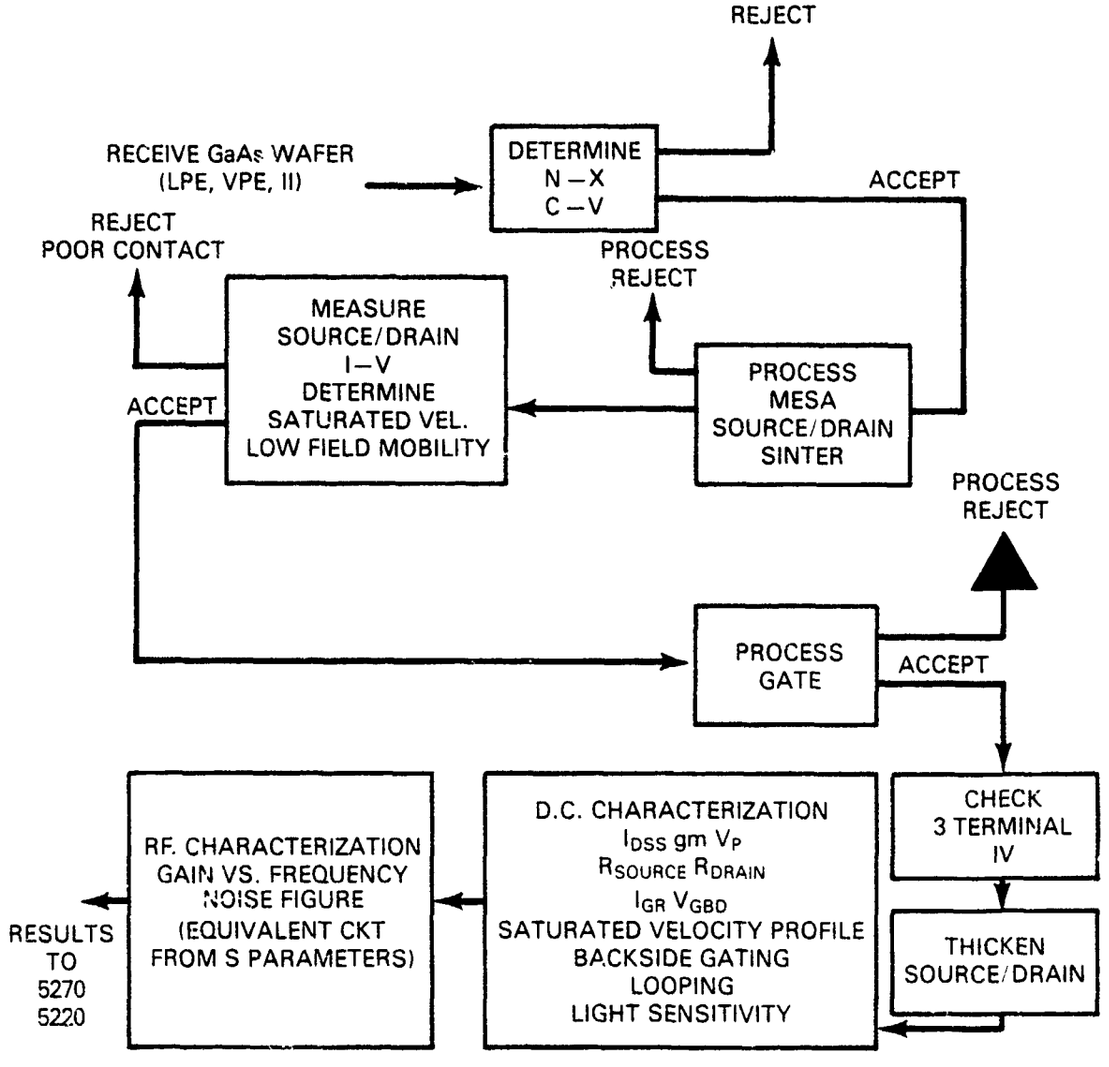

Fig. 6 -- FET processing and characterization performed by NRL Code 6811

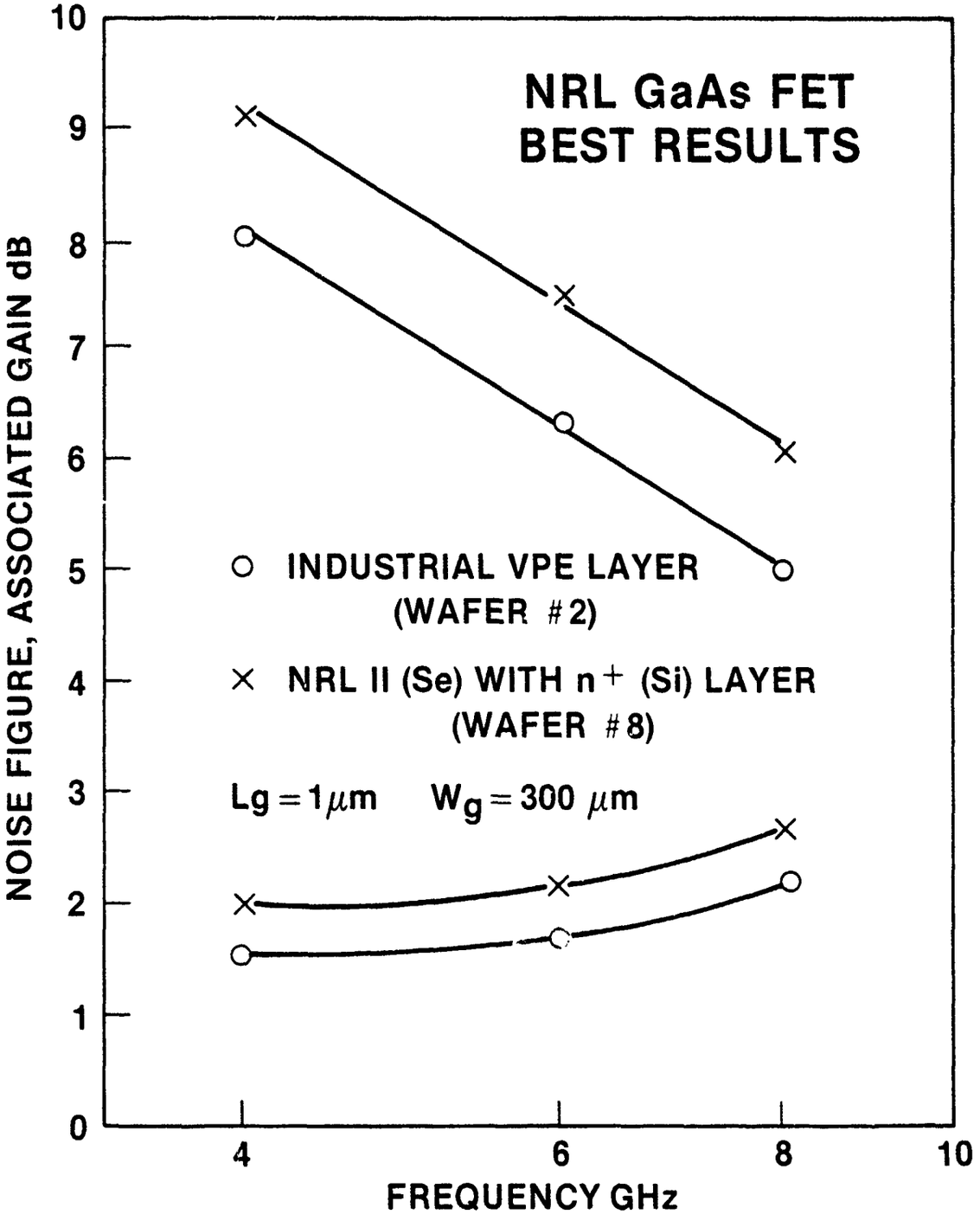

Fig. 7 — Microwave small signal performance of NRL GaAs FETs. Best results are shown.

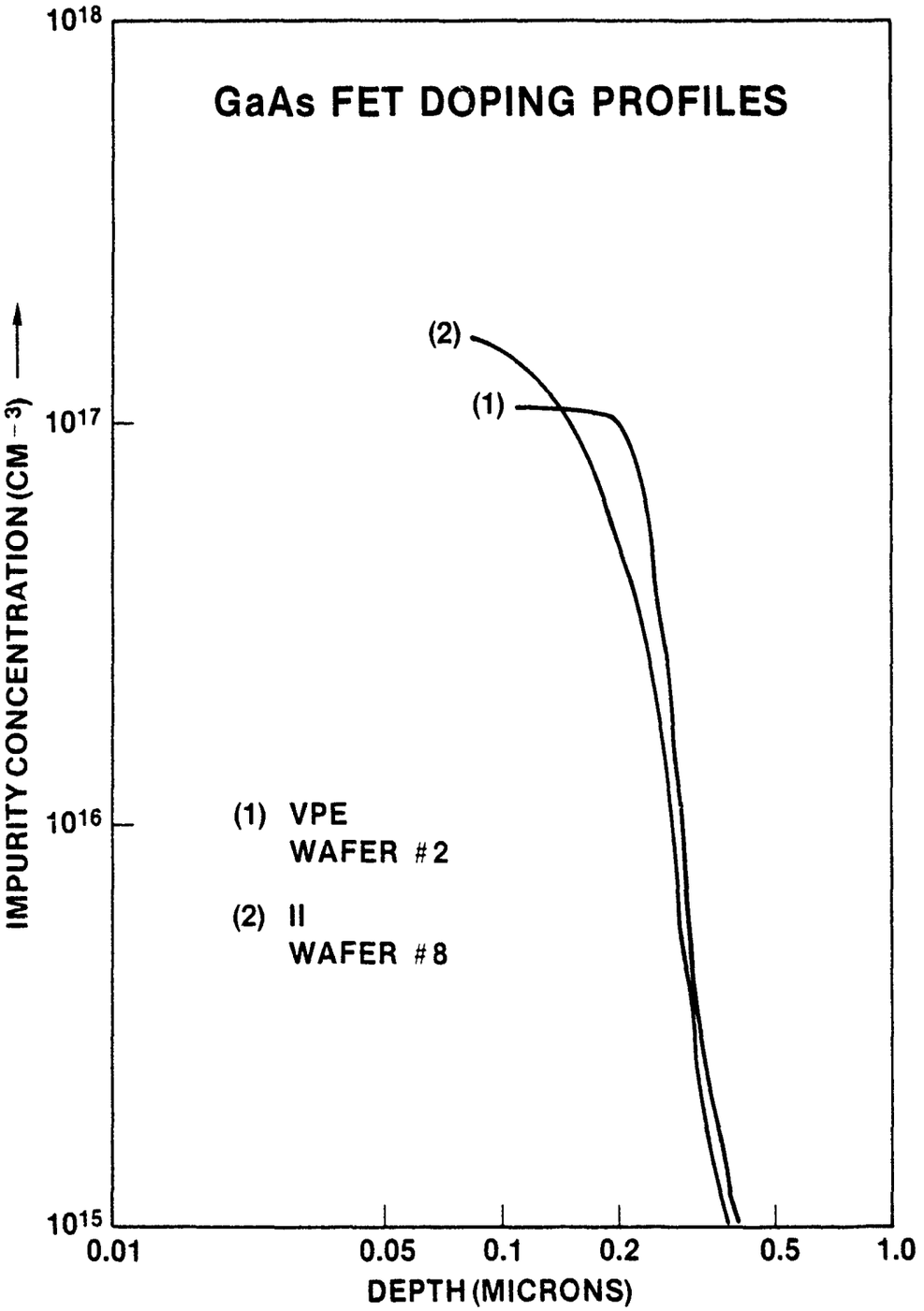

Fig. 8 — N/X profiles obtained from test patterns on wafers which gave FET microwave performance shown in Fig. 7. Ion implanted wafer represents a total NRL effort: material growth, ion implantation, and FET processing.

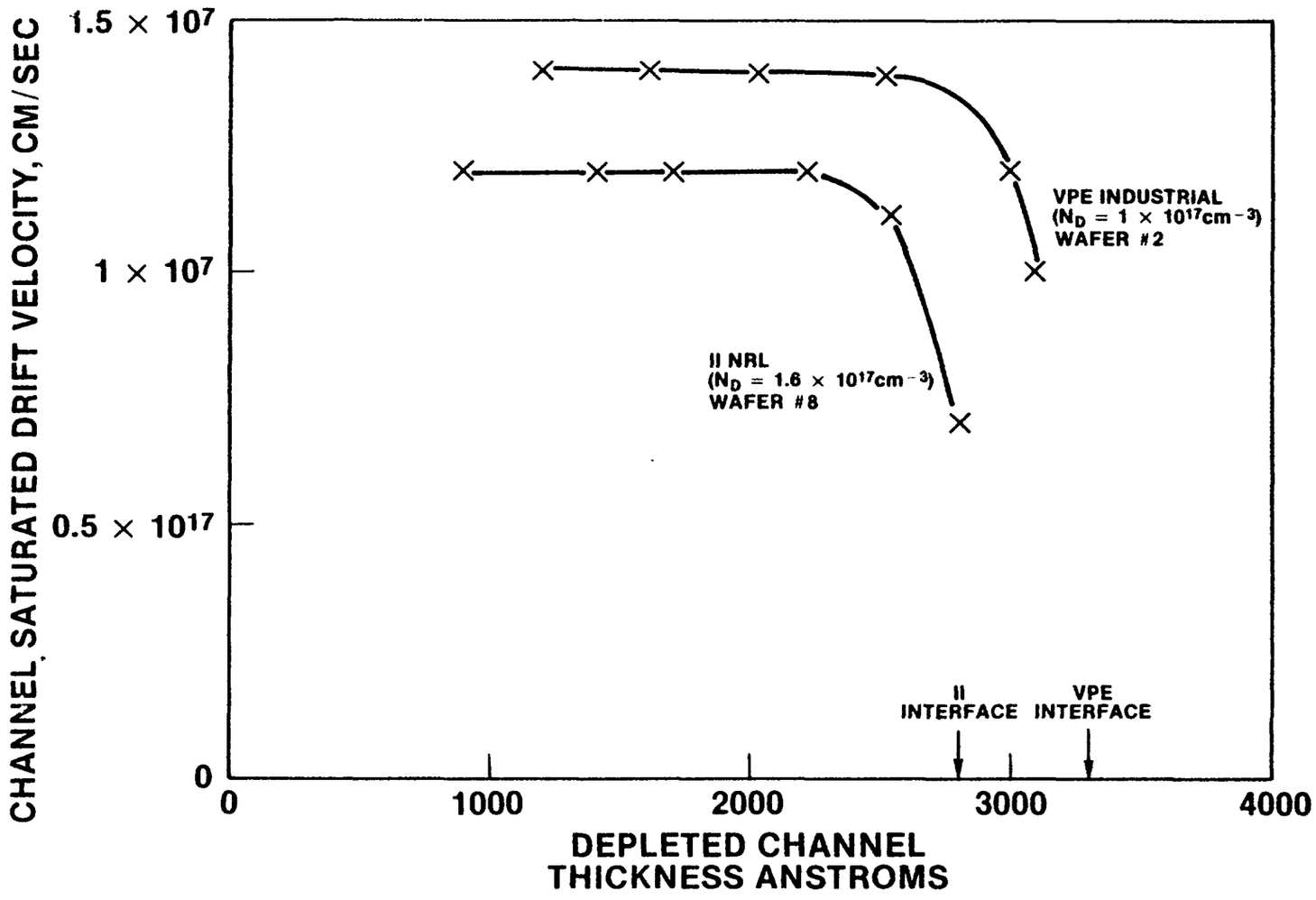

Fig. 9 — Saturated drift velocity profiles obtained from FETs whose microwave performance is depicted in Fig. 7. The region of degraded velocity is about 400Å for both types of FETs.